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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/717,917	11/21/2003	Toshihide Tsubata	1035-482	7569

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EXAMINER	
SHERMAN, STEPHEN G	

ART UNIT	PAPER NUMBER
2629	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/717,917	TSUBATA ET AL.	
	Examiner	Art Unit	
	STEPHEN G. SHERMAN	2629	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *06 February 2009*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,3-9,19-21,25,33,34, 36 and 38-41* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *21,25,33,34,40 and 41* is/are allowed.

6)☒ Claim(s) *1,3-9,20,36 and 39* is/are rejected.

7)☒ Claim(s) *19 and 38* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *20 December 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. This office action is in response to the amendment filed 6 February 2009. Claims 1 and 3-9, 19-21, 25, 33-34, 36 and 38-41 are pending.

Response to Arguments

2. Applicant's arguments with respect to claims 1, 3-9, 20, 36 and 39 have been considered but are moot in view of the new ground(s) of rejection.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.

4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

5. Claims 1, 4, 6, 8, 20 and 39 are rejected under 35 U.S.C. 103(a) as being unpatentable over AAPA (Page 1, line 8, to page 9, line 2 of the specification and Figures 12 and 13.) in view of Morita et al. (US 6,259,200).

Regarding claim 1, AAPA disclose a display device substrate (Figure 13, 110), comprising:

one or more pixel electrodes each of which is provided on each intersection of a signal line and a scanning line that are provided on an insulating substrate (Figures 12 and 13 shows that pixel electrode 103' is located at the intersection of scanning line 104 and signal line 102, and are provided on substrate 110, which is explained to be insulating on page 5, lines 16-20.); and

an interlayer insulating film stacked between the signal line and the pixel electrode (Figure 13 shows interlayer insulating film layer 115 between the signal line 102 and the pixel electrode 103'.), wherein

in view of a vertical direction with respect to a surface of the insulating substrate, the signal line is provided on an area on which the pixel electrode is not provided (Figure 13 shows that there is a gap between pixel electrodes 103' and 103, and that the signal line 102 is provided on this area, and thus the signal line is provided on an area on which the pixel electrode is not provided.); and

wherein the signal line is covered by a light shielding film having an insulating property that contacts the signal line (Figure 13 shows that light shielding film 108 contacts the signal line 102.);

wherein the interlayer insulating film is provided on the light shielding film (Figure 13 shows that the interlayer film 115 is provided on the light shielding film 108.);

wherein the pixel electrode is provided on the interlayer insulating film (Figure 13 shows that the pixel electrode 103' is provided on the interlayer film 115.); and

wherein in view of a vertical direction with respect to the surface of the insulating substrate, a surface of the signal line is covered by the light shielding film (Figure 13 shows that in view of the vertical direction that the signal line 102 is covered by the light shielding film 108.),

wherein in view of a vertical direction with respect to a surface of the insulating substrate, the pixel electrode, the interlayer insulating film, the light-shielding film, and the signal line are provided in this order (Figure 13 shows that the order provided is pixel electrode 103', then interlayer film 115, then light shielding film 108 then the signal line 102.); and

wherein no voltage is applied to a region between the pixel electrode and the signal line (Figure 13, where since the light shielding film 108 is insulating, there is no voltage applied to the area between the pixel electrode and the signal line.).

AAPA fail to teach that a gap is provided between the signal line and the pixel electrode.

Morita et al. disclose a display device substrate in which a gap is provided between the signal line and the pixel electrode (Column 4, lines 44-50).

Therefore, it would have been obvious to "one of ordinary skill" in the art at the time the invention was made to make a gap as taught by Morita et al. between the signal line and pixel electrode taught by AAPA in order to reduce stray capacitance formed between the signal lien and pixel electrode, where in this combination, the gap will be covered by the light shielding film and include an area in which no voltage is applied.

Regarding claim 4, AAPA and Morita et al. disclose the display device substrate as set forth in claim 1.

Morita et al. also disclose a display device substrate further comprising:

an active element provided on each intersection of the signal line and the scanning line (Figure 8 shows the TFT 3 found at the intersection.);

the light shielding film provided so as to cover at least a surface of the signal line among the signal line, the active element, and the scanning line (Figure 2 shows light shielding film 5 covering at least a surface of the signal line 10.), wherein

in view of the vertical direction with surface of the insulating substrate, respect to the a gap between the pixel electrodes which are adjacent to each other with the signal line there between is covered by the light shielding film (As explained above, there is a gap in the vertical direction between the pixel electrodes 14 with the signal line 10 in between and covered by the light shielding film 5.).

Regarding claim 6, AAPA and Morita et al. disclose the display device substrate as set forth in claim 1.

Morita et al. also disclose a display device substrate further comprising:

an active element provided on each intersection of the signal line and the scanning line (Figure 8 shows the TFT 3 found at the intersection.); and

the light shielding film provided so as to cover at least a surface of the signal line among the signal line, the active element, and the scanning line (Figure 2 shows light shielding film 5 covering at least a surface of the signal line 10.), wherein

in view of the vertical direction with respect to the surface of the insulating substrate, (i) the light shielding film which covers the surface of the signal line film and (ii) the pixel electrode overlap with each other (As explained above the light shielding film 5 which covers the signal line 10 overlaps with the pixel electrode 14 as well.).

Regarding claim 8, AAPA and Morita et al. disclose the display device substrate as set forth in claim 1.

Morita et al. also disclose a display device substrate further comprising:

an active element provided on each intersection of the signal line and the scanning line (Figure 8 shows the TFT 3 found at the intersection.);

a contact hole for allowing the active element and the pixel electrode to be in contact with each other (Figure 6, element 8 shows the contact hole.); and

a light shielding film provided so as to cover surfaces of the active element, the signal line, and the scanning line (Figure 6 shows light shielding film 62.), wherein

in view of the vertical direction with respect to the surface of the insulating substrate, (i) the light shielding film which covers the surface of the signal line film and (ii) the pixel electrode overlap with each other (As explained above the light shielding film 5 which covers the signal line 10 overlaps with the pixel electrode 14 as well.).

Regarding claim 20, AAPA and Morita et al. disclose a liquid crystal display device, comprising the display device substrate as set forth in claim 1 (Figure 7 of Morita et al.).

Regarding claim 39, AAPA and Morita et al. disclose a display device substrate as set forth in claim 1, wherein the interlayer insulating film contacts the light shielding film and the pixel electrode contacts the interlayer insulating film (AAPA, Figure 13 shows that the interlayer film 115 and the light shielding film 108 contact each other, and that the pixel electrode 103' contacts the interlayer film 115.).

6. Claims 3, 5, 7 and 9 are rejected under 35 U.S.C. 103(a) as being unpatentable over AAPA (Page 1, line 8, to page 9, line 2 of the specification and Figures 12 and 13.) in view of Morita et al. (US 6,259,200) and further in view of Zhang et al. (US 6,396,470).

Regarding claims 3, 5, 7 and 9, AAPA and Morita et al. disclose the display device substrate as set forth in claims 2, 4, 6, 8, 10, 13 and 16.

Morita et al. and AAPA fail to teach wherein the light shielding film is made of resin having an insulating property.

Zhang et al. disclose of a light shielding film made of resin having an insulating property (Column 12, lines 54-63 explain that the light shielding film shown in Figure 8 is an insulating black resin.).

Therefore it would have been obvious to "one of ordinary skill" ion the art at the time the invention was made that the light shielding film taught by the combination of AAPA and Morita et al. be made of an insulating resin as taught by Zhang et al. in order to allow the light shielding film to be formed in a desired area without using a resist mask.

7. Claim 36 is rejected under 35 U.S.C. 103(a) as being unpatentable over AAPA (Page 1, line 8, to page 9, line 2 of the specification and Figures 12 and 13.) in view of Morita et al. (US 6,259,200) and further in view of Sato (US 5,446,562).

Regarding claim 36, AAPA and Morita et al. disclose the display device substrate as set forth in claim 1.

AAPA and Morita et al. fail to teach wherein the gap is provided between the signal line and the pixel electrode for reducing parasitic capacitance between the pixel electrode and the signal line.

Sato discloses from column 1, line 59 to column 2, line 11 that when the gap between the pixel electrode and the signal line is narrow, there is a problem of a coupling capacitance/crosstalk and disorder of the orientation of the liquid crystal, i.e. display unevenness, and also explain that the display unevenness is related to capacitance between the pixel electrode and signal line and effects the pixel potential.

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made it apply the teachings of Sato to the device taught by the combination of AAPA and Morita et al., such that the gap taught by Morita et al. is optimized to reduce the capacitance.

Allowable Subject Matter

8. Claims 21, 25, 33-34 and 40-41 are allowed.

9. The following is a statement of reasons for the indication of allowable subject matter:

The primary reason for indicating allowable subject mater is the inclusion of the limitation "wherein a size of the gap is related to a desired ΔΔβ value which is interrelated with display unevenness, the ΔΔβ value in turn being related to a difference in parasitic capacitance between the pixel electrode and the signal line and affecting a difference in an effective Value (Vd) of pixel potential of the pixel electrode; wherein an upper limit of the size of the gap is 15 μm: and wherein the desired ΔΔβ value is not

more than 0.08" as claimed in independent claim 21 and "wherein in width the gap is not less than 1 μm and not more than a value at which display unevenness is not sufficiently improved relative to aperture ratio; wherein an upper limit of the width of the gap is 15 μm;" as claimed in independent claim 33, which define the limitations of the size of the gap, which is not found singularly or in combination within the prior art.

10. Claims 19 and 38 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

The objection to claims 19 and 38 are for similar reasons as those stated above for claims 21 and 33, where claims 19 and 38 define the structural size limitations for the gap.

Conclusion

11. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not

mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

12. Any inquiry concerning this communication or earlier communications from the examiner should be directed to STEPHEN G. SHERMAN whose telephone number is (571)272-2941. The examiner can normally be reached on M-F, 8:00 a.m. - 4:30 p.m..

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Amr Awad can be reached on (571) 272-7764. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Stephen G Sherman/
Examiner, Art Unit 2629

/Amr Awad/
Supervisory Patent Examiner, Art Unit 2629

5 March 2009